

embodiment, the III-nitride is an n-type GaN substrate. The method also includes forming a III-nitride epitaxial layer (e.g., an n-type GaN epitaxial layer) coupled to the III-nitride substrate (512). The III-nitride epitaxial layer has an upper surface and is characterized by a first dopant concentration, for example n-type doping. Using the homoepitaxy techniques described herein, the thickness of the first III-nitride epitaxial layer can be thicker than available using conventional techniques, for example, between about 3  $\mu\text{m}$  and about 100  $\mu\text{m}$ , more particularly, between about 1  $\mu\text{m}$  and 80  $\mu\text{m}$ .

[0054] The method further includes forming a removing a predetermined portion of the III-nitride epitaxial layer to form one or more recessed regions extending from the upper surface of the III-nitride epitaxial layer to a predetermined depth. In an embodiment, the predetermined depth is less than the thickness. The removal process can include a masking and etching process that can include physical etching components as well as chemical etching components. Additionally, the method includes regrowing a III-nitride epitaxial material in the one or more recessed regions. The regrown III-nitride epitaxial material has an upper regrowth surface substantially coplanar with the upper surface. In some embodiments, the regrown material comprises a p-type GaN epitaxial material, for example, used in fabrication of gate regions for a JFET.

[0055] In an alternative embodiment, the method also includes forming a first electrical contact to a contact region of the upper surface of the III-nitride epitaxial layer and forming a second electrical contact to a contact region of the upper regrowth surface. Thus, in some embodiments, the regrown material provides for conduction of electrical current, application of bias to other device regions, or the like. Although the III-nitride epitaxial layer is discussed in terms of a single layer, this is not required by embodiments of the present invention and the various epitaxial layers, including the regrown epitaxial material, can include sub-layers. As an example, the III-nitride layer can include a plurality of sub-layers such as a drift sub-layer, a channel sub-layer, and a source sub-layer. Thus, in these embodiments, complex epitaxial structures are provided including both multiple epitaxial layers and/or multiple layers of regrown material.

[0056] A first metallic structure can be electrically coupled to the III-nitride substrate, a second metallic structure can be electrically coupled to the III-nitride epitaxial layer, and a third metallic structure can be electrically coupled to the regrown material. Thus, in addition to electrical connectivity to the as-grown material, electrical connectivity can be provided to the regrown material. It should be noted that the various epitaxial layers, both as-grown and regrown, do not have to be uniform in dopant concentration as a function of thickness, but may utilize varying doping profiles as appropriate to the particular application.

[0057] It should be appreciated that the specific steps illustrated in FIG. 5 provide a particular method of fabricating an electronic device according to an embodiment of the present invention. Other sequences of steps may also be performed according to alternative embodiments. For example, alternative embodiments of the present invention may perform the steps outlined above in a different order. Moreover, the individual steps illustrated in FIG. 5 may include multiple sub-steps that may be performed in various sequences as appropriate to the individual step. Furthermore, additional steps may be added or removed depending on the particular applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0058] FIG. 6 is a simplified flowchart illustrating a method of fabricating a vertical JFET with regrown gate regions according to an embodiment of the present invention. In some embodiments, the vertical JFET is referred to as a controlled switching device. Referring to FIG. 6, a III-nitride substrate is provided (610). In an embodiment, the III-nitride is an n-type GaN substrate. The method also includes forming a first III-nitride epitaxial layer (e.g., an n-type GaN epitaxial layer) coupled to the III-nitride substrate (612). The first III-nitride epitaxial layer is characterized by a first dopant concentration, for example n-type doping. Using the homoepitaxy techniques described herein, the thickness of the first III-nitride epitaxial layer can be thicker than available using conventional techniques, for example, between about 3  $\mu\text{m}$  and about 100  $\mu\text{m}$ , more particularly, between about 1  $\mu\text{m}$  and 80  $\mu\text{m}$ , as appropriate to high power operation.

[0059] The method further includes forming one or more additional III-nitride epitaxial layers (e.g., a GaN-based channel layer and a GaN-based source layer) coupled to the first III-nitride epitaxial layer (614).

[0060] The method further includes removing at least a portion of the one or more III-nitride epitaxial layers to form a set of recesses extending a predetermined distance into the one or more additional III-nitride epitaxial layers (616). The set of recesses are disposed between remaining portions of the one or more additional III-nitride epitaxial layers. The removal process can include a masking and etching process that can include physical etching components as well as chemical etching components. The method also includes regrowing an epitaxial material in the set of recesses (618). The regrown epitaxial material can form a set of gate regions interspersed between and/or at least partially surrounding channel regions associated with the remaining portions of the one or more additional epitaxial layers. In some embodiments, the regrown material has a conductivity type the opposite of the conductivity type of the one or more additional III-nitride epitaxial layers. The epitaxial material has a thickness substantially equal to the predetermined distance, providing a planar regrowth surface including an upper surface of the remaining portions of the one or more additional epitaxial layers and an upper surface of the regrown epitaxial material.

[0061] The method further includes forming a drain contact electrically coupled to the III-nitride substrate (620) and forming a set of source contacts electrically coupled to the remaining portions of the one or more additional III-nitride epitaxial layers and forming a set of gate contacts electrically coupled to the epitaxial material (622). The various epitaxial layers do not have to be uniform in dopant concentration as a function of thickness, but may utilize varying doping profiles as appropriate to the particular application.

[0062] It should be appreciated that the specific steps illustrated in FIG. 6 provide a particular method of fabricating a vertical JFET with regrown gate regions according to an embodiment of the present invention. Other sequences of steps may also be performed according to alternative embodiments. For example, alternative embodiments of the present invention may perform the steps outlined above in a different order. Moreover, the individual steps illustrated in FIG. 6 may include multiple sub-steps that may be performed in various sequences as appropriate to the individual step. Furthermore, additional steps may be added or removed depending on the particular applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.